REMARKS

In the above-identified Office Action the Examiner has objected to the claims because of the term OSF. Applicant has amended Claim 1 as well as Claim 5, 6 and 13, in general conforming with the Examiner's suggestions. Accordingly, the objections are considered to be obviated.

In addition, Claim 1 has been rejected as indefinite for the use of quotation marks. The quotation marks have been deleted and the Claim is now considered definite.

Claims 1, 2, 4 and 12 have been rejected to under 35 USC §102(e) as anticipated by Hourai. Claims 7, 8 and 10-12 have been rejected by patent to Iida. Claims 5 and 6 have been rejected as being unpatentable over Hourai. Claim 3 has been rejected as unpatentable over Hourai.

Applicant has amended the claims so that now the claims should be patentable over the references of record. More particularly, Applicant has amended Claim 1 so that now it recites that temperature parameters only are adjusted, whereas in Hourai, the diameter of the oxidation induced stacking fault ring is controlled not only by the temperature gradient, but also and the pulling rate of the silicon single crystal ingot. Accordingly, Claim 1 now recites over Hourai.

With regard to Claim 2-6 and the invention received in claim 2-6 uses the G_{outer}/G_{center} as parameters. The Hourai (USP 5,954,873) invention uses the V/G value of the crystal center position and the V/G value of the outer perimeter respectively as parameters. The use of G_{outer}/G_{center} as parameters is different from the use of the V/G value of the crystal center position and the V/G value of the outer peripheral as parameters.

As stated, according to the Hourai patent, it is necessary to control the temperature gradient G and the pulling speed V, whereas in the invention in claims 2-6, only the temperature gradient G in the pulling axis direction is controlled. As a concrete example, an embodiment is described in the specification in which the distance h from the heat-shield member to the silicon

melt is adjusted. According to the invention in claims 2-6, it is possible to control $G_{outer/}G_{center}$ regardless of the pulling speed, and a desired silicon single crystal ingot can be obtained.

Luter (USP 5,922,127) only describes the heat-shield member (shield 40) but does not describe the use of $G_{outer/}G_{center}$ as parameters.

The invention in claims 7-10 uses $G1_{edge/}G1_{center}$ as parameters. The Iida (USP 5,986,264) patent uses ΔG=Ge-Gc (corresponding to the $G1_{edge/}G1_{center}$ of the present invention), that is, the in-furnace temperature is adjusted so that ΔG is controlled to be within 5°C/cm. The use of $G1_{edge/}G1_{center}$ as parameters is different from the use of the G1e/G1c (corresponding to the $G1_{edge/}G1_{center}$ of the present invention) as parameters.

The defect seed in the crystal is determined from the V/G1 value and the distribution of the defect seeds in the diameter direction is determined by the value of $((V/G1_{edge/}((V/G1_{center})$ (= assumed to be R) and the value of $(V/G1)_{center}$ of the crystal center. Here, considering one crystal, since the pulling speed V is identical for the edge and the center, it can be expressed as

$R= G1_{edge/}G1_{center} \rightarrow$ Gle/Glc...(1)

When Gle/Glc=k is used as a parameter, then it can be expressed as Gle=k·Glc...(2) When substituting the equation (2) for the equation (1), it becomes R= (k·Glc)/Glc=k... (3) which holds the relationship R=k.

The Iida invention uses ΔG= Gle-Glc = d as a parameter. In this case, it can be expressed as Gle = d+Glc ...(4)

When substituting the equation (4) for the equation (I), it becomes R= (d+Glc)/G1e= 1+ (d/Glc)...5 which does not hold the relationship R=d.

According to the present invention. because the value of R is determined regardless of the temperature gradient Glc on the crystal center axis, it is possible to determine the distribution of

defect seeds by Gle/Glc. However, the defect seed in the center portion is determined by the absolute value of Glc which is expressed by the oxidation induced stacking fault ring (inner diameter/crystal diameter) in the present invention.

According to the teachings of value of Iida, the value of R varies depending on G1c. Even when d is identical, R becomes large when Glc is small. Therefore, it can be said that the difference between the character of the defect seed in the center portion and the character of the defect seed in the periphery portion becomes large. Thus, the value of R greatly changes according to the environmental change in the furnace, e.g., alteration of in-furnace carbon parts, etc., or the pulling speed.

Applicant hereby respectfully requests reconsideration and reexamination thereof.

As a result of the above amendments, the claims are now considered allowable. With the above amendments and remarks, this application is considered ready for allowance and applicant earnestly solicits an early notice of same. Should the Examiner be of the opinion that a telephone conference would expedite prosecution of the subject application, he is respectfully requested to call the undersigned at the below-listed number.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (amended) A method for producing a silicon single crystal ingot by the Czochralski method, characterized in that by adjusting temperature parameters only during pulling of the silicon single crystal ingot, and performing pulling of ["]a silicon single crystal ingot containing a perfectly crystalline part["] such that an [OSF] oxidation induced stacking fault ring appears at a prescribed position in the silicon single crystal ingot, a production efficiency of ["]a perfectly crystalline part of the silicon single crystal ingot["] and/or of ["]a part of the silicon single crystal ingot which can be used as wafers["] is improved.

5. (amended) A silicon single crystal wafer, obtained from the silicon single crystal ingot of claim 2, wherein there exists an [OSF] oxidation induced stacking fault ring an inner diameter of which is 70% or less of an overall diameter, and in which there exists, surrounding the [OSF] oxidation induced stacking fault ring, a defect free zone occupying 50% or more of a total surface area [(]on one side[)].

6. (amended) A silicon single crystal wafer, obtained from the silicon single crystal ingot of claim 2, wherein there exists an [OSF] oxidation induced stacking fault ring an inner diameter of which is 50% or less of an overall diameter, and in which there exists, surrounding the [OSF] oxidation induced stacking fault ring, a defect free zone occupying 75% or more of a total surface area [(]on one side[)].

10. (amended) A silicon wafer for non-annealing, cut from a silicon ingot produced by the CZ method, [characterized in that] wherein the silicon ingot is produced by pulling under a condition such that $1.15 < G1_{edge}/VG1_{center} < 1.25$ an inner diameter of an [OSF] oxidation induced stacking fault ring is at least 1/2 a wafer inner diameter.

13. (amended) In a silicon wafer cut from a silicon ingot produced by the CZ method, a method to improve a gate oxide integrity in an area on the inside of an [OSF] oxidation induced stacking fault ring by controlling a ratio of an [OSF] oxidation induced stacking fault ring inner diameter to a crystal diameter, G1xG2, and $G1_{edge}/G1_{center}$.